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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,983	07/30/2003	Hideharu Koike	500-002	7730

7590 06/03/2005

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Sm

Office Action Summary	Application No.	Applicant(s)	
	10/630,983	KOIKE, HIDEHARU	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-14* is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 05/10/05 has been reviewed and considered with the following results:

As to the rejection to claims 7-14, under 35 U.S.C. 112, 1st paragraph, Applicant's clarification has overcome the rejections, as such; the rejection has been withdrawn.

As to the rejection to claims 13 and 14, under 35 U.S.C. 112, 2nd paragraph, Applicant's amendment and clarification has overcome the rejections, as such; the rejection has been withdrawn.

As to the prior art rejections to claims, Applicant's arguments with respect to the prior art rejections mailed on 02/11/2005 have been fully considered and found persuasive, as such, the prior art rejections have been withdrawn. A new action on the merits appears below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuchi (US Pat. 6,121,813).

With regard to claim 1, Furuchi discloses in Fig. 3 an integrated circuit comprising a CMOS inverter (101), the output of the CMOS inverter being coupled with an input buffer (102);

a first capacitor (10) being inserted between the output of the CMOS inverter and a first voltage source (Vdd); a second capacitor (11) being inserted between the output of the CMOS inverter and a second voltage source (ground). Fig. 3 of Furuchi shows a circuit meeting all of the claimed limitations except that the input of the CMOS inverter being coupled with an input terminal (1) instead of an input pad as recited in the claim. However, one of ordinary skill in the art would infer that both input pad and input terminal, of the CMOS inverter above, is just simply an input node to the CMOS inverter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize the circuit of Furuchi wherever it needed most including at the input pad, for the expected advantage of being able to reduce noise at that input node, which are in each case optimally matched to its application.

With regard to claims 2 and 3, the above discussed circuit of the references meets all of the claimed limitations except that Furuchi does not disclose that the integrated circuit is a LSI or a VLSI. However, it would have been obvious to one of ordinary skill in the art to realize that any integrated circuit (many types of which are well known in the art including a LSI or a VLSI as recited in the claims) can benefit from the circuit taught by the references for the advantage of being able to improve the surge protection function of the integrated circuit. Therefore, the claimed invention does not define patentably over the circuitry of the references.

With regard to claims 5 and 6, the references also meet the recited limitations in these claims.

4. Claim 4 remains rejected, as per the previous office action, under 35 U.S.C. 103(a) as being unpatentable over Furuchi, as applied to claim 1 above, and further in view of the admitted prior art, Fig. 1 in the present application.

With regard to claim 4, the above-discussed circuit of the references meets all of the claimed limitations except that the buffer circuit (102 in Fig. 3 of Furuchi) is not a Schmitt-trigger type buffer circuit. The admitted prior art (Fig. 1 in the present application) shows a circuit having a Schmitt trigger (14) as a buffer circuit. Since the admitted prior art and the circuit of the references are similar, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made utilize a Schmitt trigger circuit as the buffer circuit (102 in Fig. 3 of Furuchi) in the references' circuit in order to remove any noise spikes around the threshold point of its input on both the rising and falling edges of the input signal.

Allowable Subject Matter

5. Claims 7-14 are allowed.

The prior art of record fails to disclose or fairly suggest an integrated circuit (11 in instant Fig. 3), having specific structural limitations such as a transition circuit (31), the input of the transition circuit being coupled with an input pad (13) of the integrated circuit, the output of the transition circuit being coupled with an input buffer (14), the transition circuit comprising a Pch MOS transistor (311) and a Nch MOS transistor (312), the source of the Pch MOS transistor and the Nch MOS transistor being coupled with the input of the transition circuit; the drain of the Pch MOS transistor and the Nch MOS transistor being coupled with the output of the transition circuit; the gate of the Pch MOS transistor being coupled with a third voltage source (VDD/2),

the gate of the Nch MOS transistor being coupled with a fourth voltage source (VDD/2); a first capacitor (212) being inserted between the output of the transition circuit and a first voltage source (VDD); and a second capacitor (213) being inserted between the output of the transition circuit and a second voltage source (VSS), and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
May 18, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800